depositing a first metal and a second metal into the first openings and the second openings to form a first metallic layer and a second metallic layer respectively, wherein the first metallic layer and the second metallic layer are positioned over the first seed layer and the second seed layer, and the second metallic layer is partially filled into the second patterned opening in the second mask layer;

removing the first mask layer and the second mask layer;

forming a third mask layer over the first seed layer and the first metallic layer and forming a fourth mask layer over the second seed layer and the second metallic layer, wherein the third mask layer has a plurality of third patterned openings that exposes the first seed layer and the first metallic layer;

forming a plurality of circuit lines inside the third patterned openings such that the circuit lines are positioned over the first seed layer and the first metallic layer;

removing the third mask layer and the fourth mask layer;

removing the exposed first seed layer and the second seed layer;

forming a first solder mask layer and a second solder mask layer on the first insulating layer and the second insulating layer, wherein the first solder mask layer and the second solder mask layer has a plurality of first solder mask openings and a plurality of second solder mask openings, and the first solder mask openings at least expose a portion of the circuit lines and the second solder mask openings expose the second metallic layer;

forming a third seed layer on the first solder mask layer, in the first solder mask openings and on the circuit lines exposed by the first solder mask openings and forming a

fourth seed layer on the second solder mask layer and on the second metallic layer;

forming a fifth mask layer over the third seed layer such that the fifth mask layer has a plurality of fourth patterned openings that exposes the first solder mask openings and forming a sixth mask layer over the fourth seed layer;

forming a plurality of contacts inside the first solder mask openings above the third seed layer such that the contacts and the circuit lines are electrically connected;

removing the third mask layer and the fourth mask layer; and

removing the exposed third seed layer and the fourth seed layer.

Claim 2 (original) The substrate fabrication process of claim 1, wherein the step of forming the first seed layer and the second seed layer on the first insulating layer and the second insulating layer is performed by an electroless plating operation.

Claim 3 (original) The substrate fabrication process of claim 1, wherein the step of forming the circuit lines inside the third patterned openings is performed by an electroplating operation.

Claim 4 (original) The substrate fabrication process of claim 1, wherein the step of forming the first solder mask layer and the second solder mask layer on the first insulating layer and the second insulating layer is performed by a screen printing operation.

Claim 5 (original) The substrate fabrication process of claim 1, wherein the step of forming the third seed layer and the fourth seed layer is performed by an electroless plating operation.

Claim 6 (original) The substrate fabrication process of claim 1, wherein the step of forming the contacts inside the first solder mask openings is performed by an electroplating operation.

Claims 7-14 (cancelled)